Attorney's Docket No.:10559-535001

REMARKS

Claims 1-21 are pending in the application. Claims 1 and 16 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 5,724,565 to Dubey et al. ("Dubey"). Claims 10-15 stand rejected under 35 U.S.C. 112 as allegedly being indefinite. Claims 2-9 and 17-21 stand objected to. In view of the amendments and remarks herein, the rejections are respectfully traversed. Reconsideration and allowance are respectfully requested.

I. Allowable subject matter

The indication of allowable subject matter is gratefully acknowledged.

II. The rejections under 35 U.S.C. 112

Claim 10 has been amended to more clearly emphasize its patentable features.

The office action alleges that claim 10 is indefinite because "the order of processing for the instruction selected from the second of the plurality of context registers is ambiguous, because selection of the address for fetching takes place after the selection of instruction for execution." (Please see page 2 of the office action).

However, the "second instruction address" that is selected from the second of the plurality of registers in the second

cycle of execution of the system does not correspond to the instruction selected from the second of said plurality of context registers in the first cycle of execution of the system.

An exemplary implementation illustrating this feature is found on page 5, lines 1-5 of the specification. "In operation, at start-up, context scheduler 60 loads an instruction address into each ECR 40a-40d on bus 65. Thereafter, during operation whenever an ECR 40a-40d becomes available, context scheduler 60 loads another instruction address for another context determined ready for execution."

That is, once the "second of the plurality of registers" becomes available, another instruction address (i.e., the second instruction address) may be loaded on the second of the plurality of registers. It may then be selected in a second cycle of execution of the system.

For at least this reason, claim 10 complies with 35 U.S.C. 112. Claims 11-15, which depend from claim 10, comply with 35 U.S.C. 112 for at least the same reasons.

III. The rejections under 35 U.S.C. 102(b)

Claims 1 and 16 stand rejected under 35 U.S.C. 102(b) as allegedly being unpatentable over Dubey.

Claim 1

Claim 1 is patentable over Dubey because Dubey neither teaches nor suggests "the fetch logic selecting the address and

the instruction substantially simultaneously for a first cycle of execution of said processor unit," as recited in claim 1.

The office action alleges that column 5, line 59 of Dubey teaches this feature of claim 1. However, column 5, lines 57-61 of Dubey teaches that "An object of this invention is an improved method and apparatus for simultaneously fetching and executing different instruction threads with one or more control and data dependencies."

That is, rather than fetch logic selecting the address and selecting the instruction substantially simultaneously, Dubey teaches simultaneously fetching and executing different instruction threads. The operations being performed simultaneously in Dubey are different than the operations being performed substantially simultaneously in claim 1. Further, the operations of Dubey are not both performed by fetch logic: Dubey teaches that instructions are executed on the processor (see, e.g., column 6, lines 43-45 of Dubey).

Since Dubey neither teaches nor suggests this feature of claim 1, claim 1 is patentable over Dubey.

Claim 16

Similarly, claim 16 is patentable over Dubey because Dubey neither teaches nor suggests a computer program stored in a computer readable medium having instructions causing a computer that executes multiple contexts to "select the first instruction

for execution in a first cycle of execution of said computer; and load a second instruction corresponding to a second instruction address stored in a second of the plurality of context registers substantially simultaneously with the selection of the first instruction," as recited in claim 16.

Again, selecting a first instruction and loading a second instruction is different than fetching and executing different instruction threads.

Since Dubey neither teaches nor suggests this feature of claim 16, claim 16 is patentable over Dubey.

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CONCLUSION

In view of the above remarks and amendments, claims 1-21 are in condition for allowance, and a notice to that effect is respectfully requested. If the Examiner has any questions regarding this response, the Examiner is invited to telephone the undersigned at (858) 678-4311.

No fees are believed due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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